IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A data processor comprising:

an instruction execution pipeline comprising N processing stages; and

an instruction issue unit capable of fetching instructions into [[said]] the instruction execution pipeline, the instructions fetched from an instruction cache associated with [[said]] the data processor, each of [[said]] the fetched instructions comprising from one to S syllables, [[said]] the instruction issue unit comprising:

a first buffer comprising S storage locations capable of receiving and storing [[said]] the ~~one to S~~ syllables associated with [[said]] the fetched instructions ~~, each of said S storage locations capable of storing one of said one to S syllables of each fetched instruction~~;

a second buffer comprising S storage locations capable of receiving and storing [[said]] the ~~one to S~~ syllables associated with [[said]] the fetched instructions ~~, each of said S storage locations capable of storing one of said one to S syllables of each fetched instruction~~; and

a controller capable of:

determining if a first one of [[said]] the [[S]] storage locations in [[said]] the first buffer is full;

~~, wherein said controller,~~ in response to a determination that [[said]] the first one of [[said]] the [[S]] storage locations in the first buffer is full, ~~causes~~ causing a corresponding syllable in an incoming fetched instruction to be stored in a corresponding one of

[[said]] the [[S]] storage locations in [[said]] the second buffer;

~~, wherein at least one of the one to S syllables in the first buffer is transferred into at least one of a plurality of issue lanes leading into the instruction execution pipeline, and wherein the controller is capable of~~ using a stop bit in a highest syllable of one of the instructions to determine whether every syllable of the instruction has been stored in the first buffer; and

in response to a determination that every syllable of one of the instructions has been stored in the first buffer, causing the syllables of the instruction to be transferred from the first buffer into at least one of a plurality of issue lanes leading into the instruction execution pipeline;

wherein the instruction issue unit is capable of fetching syllables from multiple cache lines of the instruction cache during a single fetch.

2. (Original) The data processor as set forth in Claim 1 wherein S=4.

3. (Original) The data processor as set forth in Claim 1 wherein S=8.

4. (Original) The data processor as set forth in Claim 1 wherein S is a multiple of four.

5. (Currently Amended) The data processor as set forth in Claim 1 wherein each of ~~said one to S~~ the syllables comprises 32 bits.

6. (Currently Amended) The data processor as set forth in Claim 1 wherein each of ~~said one to S~~ the syllables comprises 16 bits.

7. (Currently Amended) The data processor as set forth in Claim 1 wherein each of ~~said one to S~~ the syllables comprises 64 bits.

8. (Cancelled).

9. (Currently Amended) The data processor as set forth in Claim [[8]] 1 wherein [[said]] the controller is further capable of:

determining if [[a]] the syllable in [[said]] the first one of [[said]] the [[S]] storage locations in [[said]] the first buffer has been transferred from [[said]] the first buffer to [[said]] the instruction pipeline; and ~~, wherein said controller,~~

in response to a determination that [[said]] the syllable in the first one of [[said]] the [[S]] storage locations has been transferred, ~~causes said~~ causing the corresponding syllable stored in [[said]] the corresponding one of [[said]] the [[S]] storage locations in [[said]] the second buffer to be transferred to [[said]] the first one of [[said]] the [[S]] storage locations in [[said]] the first buffer.

10. (Currently Amended) The data processor as set forth in Claim 9 further comprising a switching circuit controlled by [[said]] the controller and operable to transfer syllables from [[said]] the second buffer to [[said]] the first buffer.

11. (Currently Amended) A processing system comprising:

a data processor comprising:

an instruction execution pipeline comprising N processing stages; and

an instruction issue unit capable of fetching instructions into [[said]] the instruction execution pipeline, the instructions fetched from an instruction cache associated with [[said]] the data processor, each of [[said]] the fetched instructions comprising from one to S syllables, [[said]] the instruction issue unit comprising:

a first buffer comprising S storage locations capable of receiving and storing [[said]] the ~~one to S~~ syllables associated with [[said]] the fetched instructions ~~, each of said S storage locations capable of storing one of said one to S syllables of each fetched instruction~~;

a second buffer comprising S storage locations capable of receiving and storing [[said]] the ~~one to S~~ syllables associated with [[said]] the fetched instructions ~~, each of said S storage locations capable of storing one of said one to S syllables of each fetched instruction~~; and

a controller capable of:

determining if a first one of [[said]] the [[S]] storage locations in [[said]] the first buffer is full;

~~, wherein said controller,~~ in response to a determination that [[said]] the first one of [[said]] the [[S]] storage locations in the first buffer is full, ~~causes~~ causing a corresponding syllable in an incoming fetched instruction to be stored in a corresponding one

of [[said]] the [[S]] storage locations in [[said]] the second buffer;

~~, wherein at least one of the one to S syllables in the first buffer is transferred into at least one of a plurality of issue lanes leading into the instruction execution pipeline, and wherein the controller is capable of~~ using a stop bit in a highest syllable of one of the instructions to determine whether every syllable of the instruction has been stored in the first buffer; and

in response to a determination that every syllable of one of the instructions has been stored in the first buffer, causing the syllables of the instruction to be transferred from the first buffer into at least one of a plurality of issue lanes leading into the instruction execution pipeline;

a memory coupled to [[said]] the data processor; and

a plurality of memory-mapped peripheral circuits coupled to [[said]] the data processor for performing selected functions in association with [[said]] the data processor;

wherein the instruction issue unit is capable of fetching syllables from multiple cache lines of the instruction cache during a single fetch.

12. (Original) The processing system as set forth in Claim 11 wherein S=4.

13. (Original) The processing system as set forth in Claim 11 wherein S=8.

14. (Original) The processing system as set forth in Claim 11 wherein S is a multiple of four.

15. (Currently Amended) The processing system as set forth in Claim 11 wherein each of ~~said one to S~~ the syllables comprises 32 bits.

16. (Currently Amended) The processing system as set forth in Claim 11 wherein each of ~~said one to S~~ the syllables comprises 16 bits.

17. (Currently Amended) The processing system as set forth in Claim 11 wherein each of ~~said one to S~~ the syllables comprises 64 bits.

18. (Cancelled).

19. (Currently Amended) The processing system as set forth in Claim [[18]] 11 wherein [[said]] the controller is further capable of:

determining if [[a]] the syllable in [[said]] the first one of [[said]] the [[S]] storage locations in [[said]] the first buffer has been transferred from [[said]] the first buffer to [[said]] the instruction pipeline; and ~~, wherein said controller,~~

in response to a determination that [[said]] the syllable in the first one of [[said]] the [[S]] storage locations has been transferred, ~~causes said~~ causing the corresponding syllable stored in [[said]] the corresponding one of [[said]] the [[S]] storage locations in [[said]] the second buffer to be transferred to [[said]] the first one of [[said]] the [[S]] storage locations in [[said]] the first buffer.

20. (Currently Amended) The processing system as set forth in Claim 19 further comprising a switching circuit controlled by [[said]] the controller and operable to transfer syllables from [[said]] the second buffer to [[said]] the first buffer.

21. (Currently Amended) For use in a data processor comprising an instruction execution pipeline having ~~comprising~~ N processing stages, a method of fetching instructions into the instruction execution pipeline ~~instructions fetched from an instruction cache associated with the data processor~~, each of the fetched instructions comprising from one to S syllables, the method ~~of fetching~~ comprising the steps of:

fetching syllables from an instruction cache associated with the data processor, wherein fetching the syllables comprises fetching syllables from multiple cache lines of the instruction cache during a single fetch;

storing at least one of the fetched syllables in a first buffer, the first buffer comprising S storage locations ~~the one to S syllables associated with the fetched instructions, each of the S storage locations capable of storing one of the one to S syllables of each fetched instruction~~;

determining if a first one of the [[S]] storage locations in the first buffer is full;

in response to a determination that the first one of the [[S]] storage locations in the first buffer is full, storing ~~a corresponding~~ another of the fetched syllables ~~in an incoming fetched instruction~~ in a corresponding ~~one of S~~ storage location [[s]] in a second buffer, wherein the second buffer comprises S storage locations ~~, each of the S storage locations in the second buffer capable of storing one of the one to S syllables of each fetched instruction~~; and

transferring at least one of the ~~one to S~~ syllables in the first buffer into at least one of a plurality of issue lanes leading into the instruction execution pipeline in response to determining that every syllable of one of the instructions has been stored in the first buffer using a stop bit in a highest syllable of the instruction.

22. (Original) The method as set forth in Claim 21 wherein S is a multiple of four.

23. (Currently Amended) The method as set forth in Claim 21 wherein each of the ~~one to S~~ syllables comprises one of: a) 16 bits, b) 32 bits, and c) 64 bits.

24. (Cancelled).

25. (Currently Amended) The method as set forth in Claim 24 further comprising the steps of:

determining if [[a]] the syllable in the first one of the [[S]] storage locations in the first buffer has been transferred from the first buffer to the instruction pipeline; and

in response to a determination that the syllable in the first one of the [[S]] storage locations in the first buffer has been transferred, transferring the corresponding syllable stored in the corresponding ~~one of the S~~ storage location [[s]] in the second buffer to the first one of the [[S]] storage locations in the first buffer.